Instruction Manual

Tektronix

TMS 104
i386DX Microprocessor Support

070-9807-00

There are no current European directives that apply to this product. This product provides cable and test lead connections to a test object of electronic measuring and test equipment.

Warning
The servicing instructions are for use by qualified personnel only. To avoid personal injury, do not perform any servicing unless you are qualified to do so. Refer to all safety summaries prior to performing service.

Printed in the U.S.A.

Tektronix, Inc., P.O. Box 1000, Wilsonville, OR 97070–1000

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In order to obtain service under this warranty, Customer must notify Tektronix of the defect before the expiration of the warranty period and make suitable arrangements for the performance of service. Customer shall be responsible for packaging and shipping the defective product to the service center designated by Tektronix, with shipping charges prepaid. Tektronix shall pay for the return of the product to Customer if the shipment is to a location within the country in which the Tektronix service center is located. Customer shall be responsible for paying all shipping charges, duties, taxes, and any other charges for products returned to any other locations.

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General Safety Summary

Review the following safety precautions to avoid injury and prevent damage to this product or any products connected to it. To avoid potential hazards, use this product only as specified.

Only qualified personnel should perform service procedures.

While using this product, you may need to access other parts of the system. Read the *General Safety Summary* in other system manuals for warnings and cautions related to operating the system.

To Avoid Fire or Personal Injury

Use Proper Power Cord. Use only the power cord specified for this product and certified for the country of use.

Use Proper Voltage Setting. Before applying power, ensure that the line selector is in the proper position for the power source being used.

Connect and Disconnect Properly. Do not connect or disconnect probes or test leads while they are connected to a voltage source.

Observe All Terminal Ratings. To avoid fire or shock hazard, observe all ratings and marking on the product. Consult the product manual for further ratings information before making connections to the product.

The common terminal is at ground potential. Do not connect the common terminal to elevated voltages.

Do not apply a potential to any terminal, including the common terminal, that exceeds the maximum rating of that terminal.

Replace Batteries Properly. Replace batteries only with the proper type and rating specified.

Recharge Batteries Properly. Recharge batteries for the recommended charge cycle only.

Use Proper AC Adapter. Use only the AC adapter specified for this product.

Do Not Operate Without Covers. Do not operate this product with covers or panels removed.

Use Proper Fuse. Use only the fuse type and rating specified for this product.

Avoid Exposed Circuitry. Do not touch exposed connections and components when power is present.

Wear Eye Protection. Wear eye protection if exposure to high-intensity rays or laser radiation exists.

Do Not Operate With Suspected Failures. If you suspect there is damage to this product, have it inspected by qualified service personnel.

Do Not Operate in Wet/Damp Conditions.

Do Not Operate in an Explosive Atmosphere.

Keep Product Surfaces Clean and Dry.

Provide Proper Ventilation. Refer to the manual's installation instructions for details on installing the product so it has proper ventilation.

Symbols and Terms

Terms in this Manual. These terms may appear in this manual:

WARNING. *Warning statements identify conditions or practices that could result in injury or loss of life.*

CAUTION. *Caution statements identify conditions or practices that could result in damage to this product or other property.*

Terms on the Product. These terms may appear on the product:

DANGER indicates an injury hazard immediately accessible as you read the marking.

WARNING indicates an injury hazard not immediately accessible as you read the marking.

CAUTION indicates a hazard to property including the product.

Symbols on the Product. The following symbols may appear on the product:

WARNING
High Voltage

Protective Ground
(Earth) Terminal

CAUTION
Refer to Manual

Double
Insulated

Service Safety Summary

Only qualified personnel should perform service procedures. Read this *Service Safety Summary* and the *General Safety Summary* before performing any service procedures.

Do Not Service Alone. Do not perform internal service or adjustments of this product unless another person capable of rendering first aid and resuscitation is present.

Disconnect Power. To avoid electric shock, disconnect the main power by means of the power cord or, if provided, the power switch.

Use Care When Servicing With Power On. Dangerous voltages or currents may exist in this product. Disconnect power, remove battery (if applicable), and disconnect test leads before removing protective panels, soldering, or replacing components.

To avoid electric shock, do not touch exposed connections.

Preface: Microprocessor Support Documentation

This instruction manual contains specific information about the TMS 104 i386DX microprocessor support and is part of a set of information on how to operate this product on compatible Tektronix logic analyzers.

If you are familiar with operating microprocessor supports on the logic analyzer for which the TMS 104 i386DX support was purchased, you will probably only need this instruction manual to set up and run the support.

If you are not familiar with operating microprocessor supports, you will need to supplement this instruction manual with information on basic operations to set up and run the support.

Information on basic operations of microprocessor supports is included with each product. Each logic analyzer has basic information that describes how to perform tasks common to supports on that platform. This information can be in the form of online help, an installation manual, or a user manual.

This manual provides detailed information on the following topics:

- Connecting the logic analyzer to the system under test
- Setting up the logic analyzer to acquire data from the system under test
- Acquiring and viewing disassembled data
- The TMS 104 i386DX probe adapter

Manual Conventions

This manual uses the following conventions:

- The term disassembler refers to the software that disassembles bus cycles into instruction mnemonics and cycle types.
- The phrase “information on basic operations” refers to online help, an installation manual, or a basic operations of microprocessor supports user manual.
- In the information on basic operations, the term XXX or P54C used in field selections and file names can be replaced with 386DX. This is the name of the microprocessor in field selections and file names you must use to operate the i386DX support.
- The term system under test (SUT) refers to the microprocessor-based system from which data will be acquired.

- The term logic analyzer refers to the Tektronix logic analyzer for which this product was purchased.
- The term module refers to a 102/136-channel, a 96-channel, or a module.
- 386DX refers to all supported variations of the i386DX microprocessor unless otherwise noted.
- A signal that is active low has a tilde (~) following its name.

Logic Analyzer Documentation

A description of other documentation available for each type of Tektronix logic analyzer is located in the corresponding module user manual. The user manual provides the information necessary to install, operate, maintain, and service the logic analyzer and associated products.

Contacting Tektronix

Product Support	For application-oriented questions about a Tektronix measurement product, call toll free in North America: 1-800-TEK-WIDE (1-800-835-9433 ext. 2400) 6:00 a.m. – 5:00 p.m. Pacific time Or, contact us by e-mail: tm_app_supp@tek.com For product support outside of North America, contact your local Tektronix distributor or sales office.
Service Support	Contact your local Tektronix distributor or sales office. Or, visit our web site for a listing of worldwide service locations. http://www.tek.com
For other information	In North America: 1-800-TEK-WIDE (1-800-835-9433) An operator will direct your call.
To write us	Tektronix, Inc. P.O. Box 1000 Wilsonville, OR 97070-1000

Getting Started

Getting Started

This chapter provides information on the following topics:

- The TMS 104 i386DX microprocessor support
- Logic analyzer software compatibility
- Your i386DX system requirements
- i386DX support restrictions
- How to connect to the system under test (SUT)

Support Description

The TMS 104 microprocessor support disassembles data from systems that are based on the Intel AMD i386DX microprocessor. The support runs on a compatible Tektronix logic analyzer equipped with a 102/136-channel moduleor a 96-channel module.

Refer to information on basic operations to determine how many modules and probes your logic analyzer needs to meet the minimum channel requirements for the TMS 104 microprocessor support.

Table 1–1 shows the microprocessors and packages from which the TMS 104 support can acquire and disassemble data.

Table 1–1: Supported microprocessors

Name	Package
Intel 80387DX	132-pin PGA
AMD 80386DX/DXL	132-pin PGA
AMD 80386DXL	132-pin PQFP

A complete list of standard and optional accessories is provided at the end of the parts list in the *Replaceable Mechanical Parts* chapter.

To use this product efficiently, you need to have the *i386DX Microprocessor User's Manual,* Intel, 1994.

Logic Analyzer Software Compatibility

The label on the microprocessor support floppy disk states which version of logic analyzer software the support is compatible with.

Logic Analyzer Configuration

To use the i386DX support, the Tektronix logic analyzer must be equipped with at least a 102/136-channel module or a 96-channel module. The module must be equipped with enough probes to acquire channel and clock data from signals in your i386DX-based system.

Refer to information on basic operations to determine how many modules and probes the logic analyzer needs to meet the channel requirements.

Requirements and Restrictions

You should review the general requirements and restrictions of microprocessor supports in the information on basic operations as they pertain to your SUT.

You should also review electrical, environmental, and mechanical specifications in the *Specifications* chapter in this manual as they pertain to your system under test, as well as the following descriptions of other i386DX support requirements and restrictions.

Table 1–2 lists the microprocessors and the system clock rate the TMS 104 product supports[1].

Table 1–2: Supported microprocessors and speeds

Microprocessor	Speed
Intel 80386DX	33 MHz
AMD 80386DX	33 MHz
AMD 80386DXL	40 MHz (PGA)
AMD 80386DXL	25 MHz (PQFP)

Configuring the Probe Adapter

The probe adapter does not require any configuration.

1 **Specification at time of printing. Contact your Tektronix sales representative for current information on the fastest devices supported.**

Connecting to a System Under Test

Before you connect to the SUT, you must connect the probes to the module. Your SUT must also have a minimum amount of clear space surrounding the microprocessor to accommodate the probe adapter. Refer to the *Specifications* chapter in this manual for the required clearances.

The channel and clock probes shown in this chapter are for a 102/136-channel module. Your probes will look different if you are using a 96-channel module.

The general requirements and restrictions of microprocessor supports in the information on basic operations shows the vertical dimensions of a channel or clock probe connected to square pins on a circuit board.

PGA Probe Adapter

To connect the logic analyzer to a SUT using a PGA probe adapter, follow these steps:

1. Turn off power to your SUT. It is not necessary to turn off power to the logic analyzer.

CAUTION. *Static discharge can damage the microprocessor, the probe adapter, the probes, or the module. To prevent static damage, handle all of the above only in a static-free environment.*

Always wear a grounding wrist strap or similar device while handling the microprocessor and probe adapter.

2. To discharge your stored static electricity, touch the ground connector located on the back of the logic analyzer. Then, touch any of the ground pins of the probe adapter to discharge stored static electricity from the probe adapter.
3. Place the probe adapter on the antistatic shipping foam to support the probe as shown in Figure 1–1. This prevents the circuit board from flexing and the socket pins from bending.
4. Remove the microprocessor from your SUT.
5. Line up the pin A1 indicator on the probe adapter board with the pin A1 indicator on the microprocessor.

CAUTION. *Failure to correctly place the microprocessor into the probe adapter might permanently damage the microprocessor once power is applied.*

6. Place the microprocessor into the probe adapter as shown in Figure 1–1.

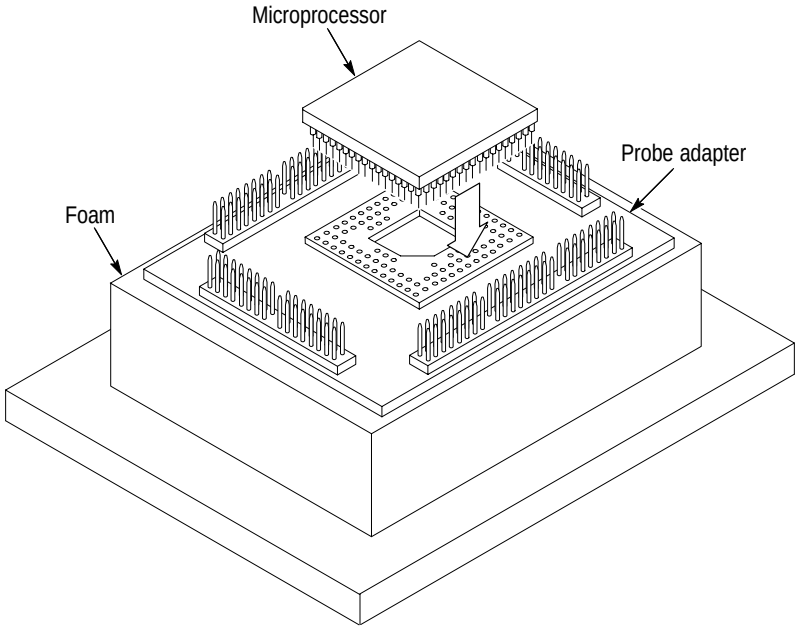


Figure 1–1: Placing a microprocessor into a PGA probe adapter

7. Connect the channel and clock probes to the probe adapter as shown in Figure 1–2. Match the channel groups and numbers on the probe labels to the corresponding pins on the probe adapter. Match the ground pins on the probes to the corresponding pins on the probe adapter.

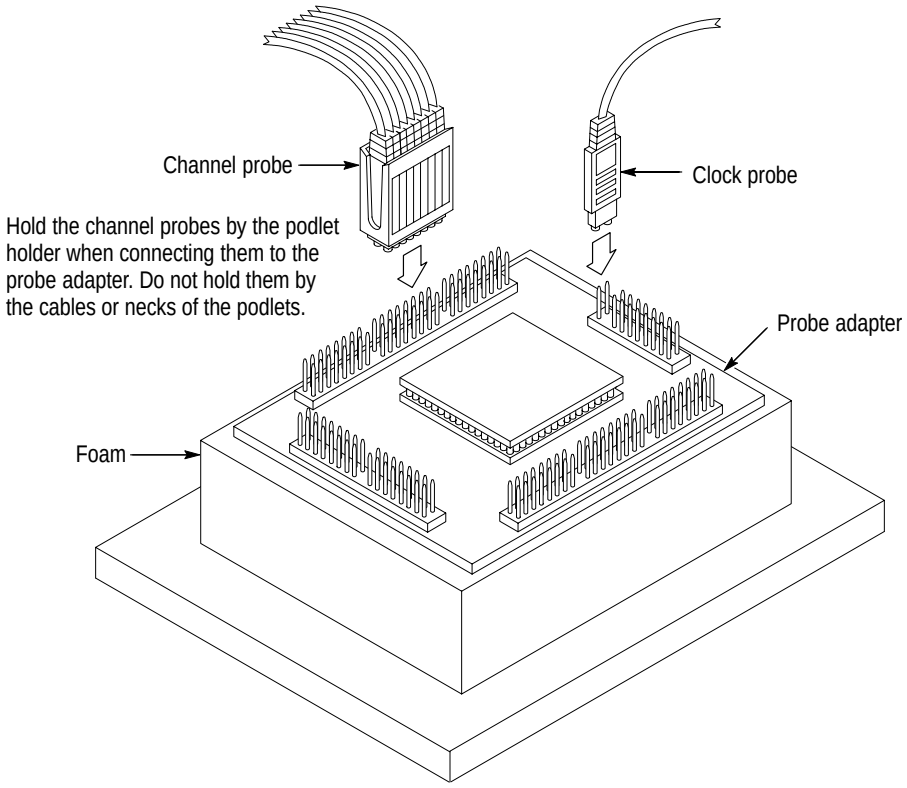


Figure 1–2: Connecting probes to a PGA probe adapter

8. Line up the pin A1 indicator on the probe adapter board with the pin A1 indicator on your SUT.

9. Place the probe adapter onto the SUT as shown in Figure 1–3.

NOTE. *You might need to stack one or more replacement sockets between the SUT and the probe adapter to provide sufficient vertical clearance from adjacent components. However, keep in mind that this might increase loading, which can reduce the electrical performance of your probe adapter.*

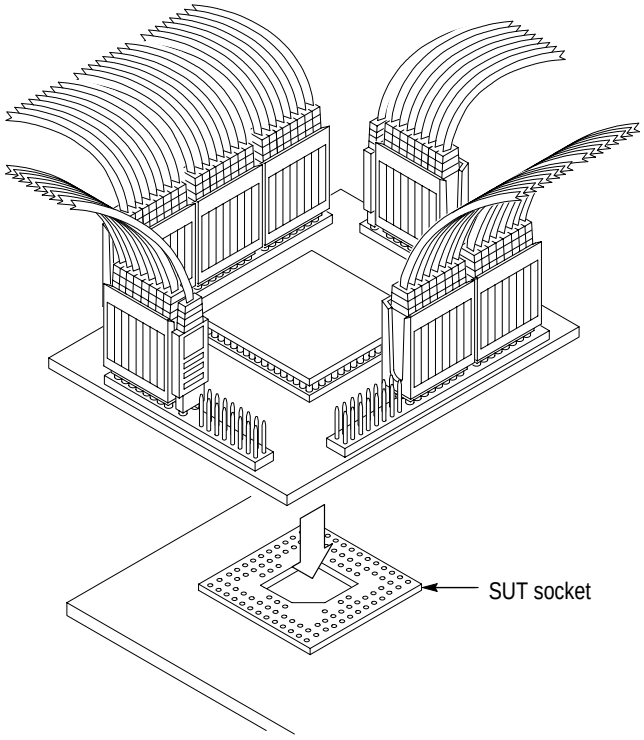


Figure 1–3: Placing a PGA probe adapter onto the SUT

PQFP Probe Adapter

To connect the logic analyzer to an SUT using a PQFP probe adapter, follow these steps:

1. Turn off power to your SUT. It is not necessary to turn off the logic analyzer.

CAUTION. *Static discharge can damage the microprocessor, the probe adapter, the probes, or the module. To prevent static damage, handle all of these only in a static-free environment.*

Always wear a grounding wrist strap or similar device while handling the microprocessor and probe adapter.

2. To discharge your stored static electricity, touch the ground connector located on the back of the logic analyzer. Then, touch any of the ground pins of the probe adapter to discharge stored static electricity from the probe adapter.
3. Place the probe adapter on the antistatic shipping foam to support the probe as shown Figure 1–4. This prevents the circuit board from flexing.
4. Connect the channel and clock probes to the probe adapter as shown in Figure 1–4. Match the channel groups and numbers on the probe labels to the

corresponding pins on the probe adapter. Match the ground pins on the probes to the corresponding pins on the probe adapter.

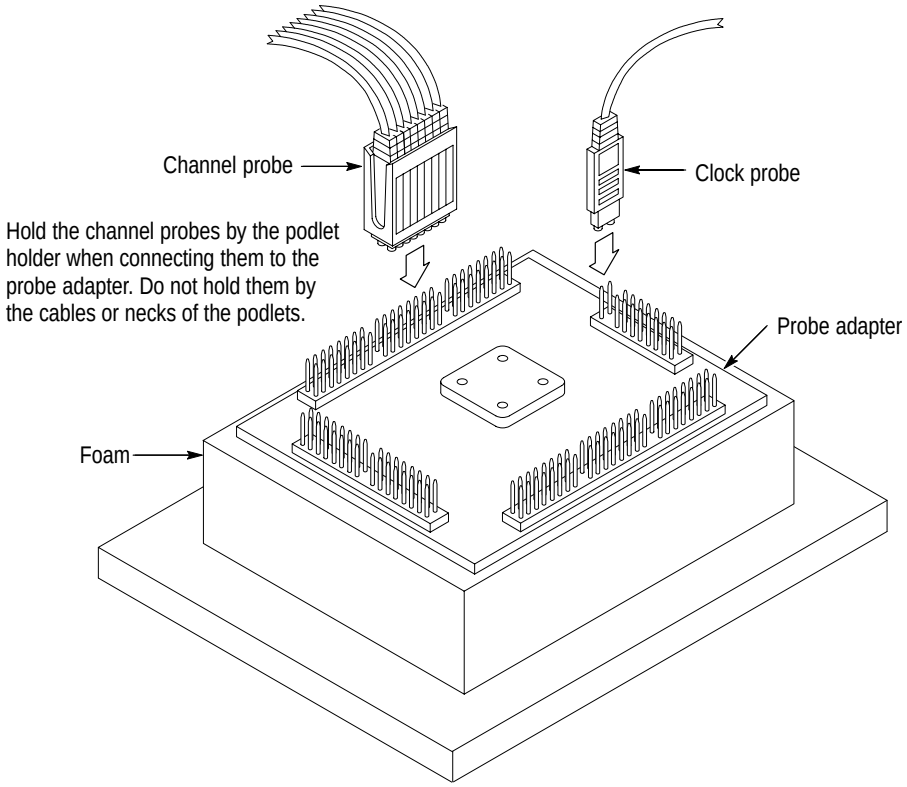


Figure 1–4: Connecting probes to a PQFP probe adapter

CAUTION. *This JEDEC PQFP (Plastic Quad Flat Pack) probe adapter has been equipped with a clip that has been designed for tight tolerances.*

The clip supports only Plastic Quad Flat Pack devices that conform to the JEDEC M0-069 October 1990 specification. Attaching the clip to a device that does not conform to this JEDEC standard can easily damage the clip's connection pins and/or the microprocessor, causing the probe adapter to malfunction.

Please contact your IC manufacturer to verify that the microprocessor you are targeting conforms to the JEDEC specification.

For best performance and long probe life, exercise extreme care when connecting the probe to the microprocessor.

5. Line up the pin 1 indicator on the microprocessor with the pin 1 indicator on the target head of the circuit board.

CAUTION. *Failure to correctly place the probe adapter onto the microprocessor might permanently damage all electrical components when power is applied.*

Center the clip on the microprocessor and apply an equal downward force on all four sides of the clip, slightly rocking the probe adapter in a clockwise circle.

Do not apply leverage to the probe adapter when installing or removing it.

6. Place the probe adapter onto the SUT as shown in Figure 1–5.

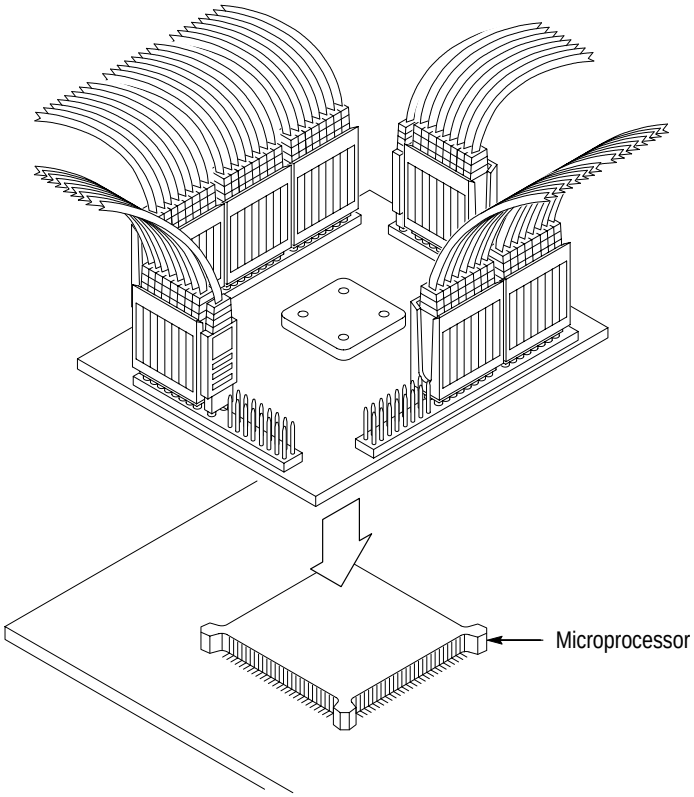


Figure 1–5: Placing a PQFP probe adapter onto the SUT

CAUTION. *The probe adapter board might slip off or slip to one side of the microprocessor because of the extra weight of the probes. This can damage the microprocessor and the SUT. To prevent this from occurring, stabilize the probe adapter by placing a non-conductive object (such as foam) between the probe adapter and the SUT.*

Without a Probe Adapter

You can use channel probes, clock probes, and leadsets with a commercial test clip (or adapter) to make connections between the logic analyzer and your SUT.

To connect the probes to i386DX signals in the SUT using a test clip, follow these steps:

1. Turn off power to your SUT. It is not necessary to turn off power to the logic analyzer.

CAUTION. *Static discharge can damage the microprocessor, the probes, or the module. To prevent static damage, handle all of these only in a static-free environment.*

Always wear a grounding wrist strap or similar device while handling the microprocessor.

2. To discharge your stored static electricity, touch the ground connector located on the back of the logic analyzer. If you are using a test clip, touch any of the ground pins on the clip to discharge stored static electricity from it.

CAUTION. *Failure to place the SUT on a horizontal surface before connecting the test clip might permanently damage the pins on the microprocessor.*

3. Place the SUT on a horizontal static-free surface.
4. Use Table 1–3 to connect the channel probes to i386DX signal pins on the test clip or in the SUT.

   Use leadsets to connect at least one ground lead from each channel probe and the ground lead from each clock probe to ground pins on your test clip.

Table 1–3: i386DX signal connections for channel probes

Section:channel	i386DX signal	Section:channel	i386DX signal
A3:7	A31	D3:7	D31
A3:6	A30	D3:6	D30
A3:5	A29	D3:5	D29
A3:4	A28	D3:4	D28
A3:3	A27	D3:3	D27
A3:2	A26	D3:2	D26
A3:1	A25	D3:1	D25
A3:0	A24	D3:0	D24
A2:7	A23	D2:7	D23

Table 1–3: i386DX signal connections for channel probes (cont.)

Section:channel	i386DX signal	Section:channel	i386DX signal
A2:6	A22	D2:6	D22
A2:5	A21	D2:5	D21
A2:4	A20	D2:4	D20
A2:3	A19	D2:3	D19
A2:2	A18	D2:2	D18
A2:1	A17	D2:1	D17
A2:0	A16	D2:0	D16
A1:7	A15	D1:7	D15
A1:6	A14	D1:6	D14
A1:5	A13	D1:5	D13
A1:4	A12	D1:4	D12
A1:3	A11	D1:3	D11
A1:2	A10	D1:2	D10
A1:1	A9	D1:1	D9
A1:0	A8	D1:0	D8
A0:7	A7	D0:7	D7
A0:6	A6	D0:6	D6
A0:5	A5	D0:5	D5
A0:4	A4	D0:4	D4
A0:3	A3	D0:3	D3
A0:2	A2	D0:2	D2
A0:1	A1_D	D0:1	D1
A0:0	A0_D	D0:0	D0
C3:7	NA_L~	C2:7	BE2~
C3:6	BS16_L~	C2:6	BE1~
C3:5	LOCK~	C2:5	CLK
C3:4	W/R~	C2:4	BE0~
C3:3	D/C~	C2:3	RESET_L
C3:2	M/I0~	C2:2	ADS~
C3:1	PIPE	C2:1	READY~
C3:0	BE3~	C2:0	HLDA
C1:7	Not connected	C0:7	same
C1:6	Not connected	C0:6	RESET

Table 1–3: i386DX signal connections for channel probes (cont.)

Section:channel	i386DX signal	Section:channel	i386DX signal
C1:5	INTR	C0:5	INTR_L
C1:4	ERROR~	C0:4	NMI_L
C1:3	same	C0:3	NA~
C1:2	same	C0:2	BS16~
C1:1	NMI	C0:1	BUSY~
C1:0	PEREQ	C0:0	HOLD

*** Signal not required for disassembly.**

Table 1–4 shows the clock probes, and the i386DX signal to which they must connect for disassembly to be correct.

Table 1–4: i386DX signal connections for clock probes

Section:channel	i386DX signal
CK:3	PIPE
CK:2	CLK
CK:1	NA_L~
CK:0	BS16_L~

5. Align pin 1 or A1 of your test clip with the corresponding pin 1 or A1 of the i386DX microprocessor in your SUT and attach the clip to the microprocessor.

Operating Basics

Setting Up the Support

This section provides information on how to set up the support. Information covers the following topics:

- Channel group definitions
- Clocking options
- Symbol table files

Remember that the information in this section is specific to the operations and functions of the TMS 104 i386DX support on any Tektronix logic analyzer for which it can be purchased. Information on basic operations describes general tasks and functions.

Before you acquire and disassemble data, load the support and specify setups for clocking and triggering as described in the information on basic operations. The support provides default values for each of these setups, but you can change them as needed.

Channel Group Definitions

The disassembler automatically defines the channel groups for the microprocessor. The channel groups for the i386DX microprocessor are Address, Data, Control, DataSize, Intr, Copr, Misc, and Misc2.

Clocking Options

The TMS 104 support offers a microprocessor-specific clocking mode for the i386DX microprocessor. This clocking mode is the default selection whenever you select the 386DX support.

(For the 102/136-channel module, from the File menu, select Load Support Package, and 386DX. For the 96-channel module, select 386DX Support in the Configuration menu.)

A description of how cycles are sampled by the module using the support and probe adapter is found in the *Specifications* chapter.

Disassembly will not be correct with the Internal or External clocking modes. Information on basic operations describes how to use these clock selections for general purpose analysis.

The clocking option for the TMS 104 support is DMA Cycles.

DMA Cycles

A DMA cycle is defined as the i386DX microprocessor giving up the bus to an alternate device (a DMA device or another microprocessor). These types of cycles are acquired when you select Included.

Symbols

The TMS 104 support supplies one symbol table file. The 386DX_Ctrl file replaces specific Control channel group values with symbolic values when Symbolic is the radix for the channel group.

Table 2–1 shows the name, bit pattern, and meaning for the symbols in the file 386DX_Ctrl, the Control channel group symbol table.

Table 2–1: Control group symbol table definitions

Symbol	Control group value RESET_L~ HLDA READY~ LOCK~ M/IO~ D/C~ W/R~	Meaning
LOCKED RD	0 0 0 0 1 1 0	Non-opcode fetch locked memory read
LOCKED WR	0 0 0 0 1 1 1	Any locked memory write
FETCH	0 0 0 X 1 0 0	Memory code read (opcode fetch)
MEM READ	0 0 0 X 1 1 0	Non-opcode fetch memory read cycle
MEM WRITE	0 0 0 X 1 1 1	Any memory write
I/O READ	0 0 0 X 0 1 0	Read from I/O port
I/O WRITE	0 0 0 X 0 1 1	Write to an I/O port
MEM RD/WR	0 0 0 X 1 1 X	Non-opcode fetch memory read or write
I/O RD/WR	0 0 0 X 0 1 X	Read from or write to an I/O port
READ	0 0 0 X X 1 0	Any memory or I/O read cycle except opcode fetch or int ack cycle
WRITE	0 0 0 X X 1 1	Any memory or I/O write
INT ACK	0 0 0 X 0 0 0	Responding to an interrupt
HALT/SHUT	0 0 0 X 1 0 1	HALT: Address=2, SHUTDOWN: Address=0
LOCKED	0 0 0 0 X X X	Inseparable back-to-back cycles
RESERVED	0 0 0 X 0 0 1	Reserved
DMA	0 1 X X X X X	Bus released to an alternate bus master
RESET	1 X X X X X X	Latched RESET signal asserted

*** Symbols used only for triggering; they are not displayed.**

Information on basic operations describes how to use symbolic values for triggering, and displaying other channel groups symbolically, such as the Address channel group.

Acquiring and Viewing Disassembled Data

This section describes how to acquire data and view it disassembled. Information covers the following topics:

- Acquiring data
- Viewing disassembled data in various display formats
- Cycle type labels
- How to change the way data is displayed
- How to change disassembled cycles with the mark cycles function

Acquiring Data

Once you load the 386DX support, choose a clocking mode and specify the trigger, you are ready to acquire and disassemble data.

If you have any problems acquiring data, refer to information on basic operations in your online help or *Appendix A: Error Messages and Disassembly Problems* in the basic operations user manual.

Viewing Disassembled Data

You can view disassembled data in four different display formats: Hardware, Software, Control Flow, and Subroutine. The information on basic operations describes how to select the disassembly display formats.

NOTE. *Selections in the Disassembly property page (the Disassembly Format Definition overlay) must be set correctly for your acquired data to be disassembled correctly. Refer to* Changing How Data is Displayed *on page 2–8.*

The default display format shows the Address, Data, and Control channel group values for each sample of acquired data.

The disassembler displays special characters and strings in the instruction mnemonics to indicate significant events. Table 2–2 shows the special characters and strings displayed by the i386DX disassembler and gives a definition of what they represent.

Table 2–2: Special characters in the display

Character or string displayed	Meaning
#	Indicates an immediate value
m	The instruction was manually marked as a program fetch
t	Indicates the number shown is in decimal, such as #12t
****	Indicates there is insufficient data available for complete disassembly of the instruction; the number of asterisks will indicate the width of the data that is unavailable. Two asterisks represent a byte.
* ILLEGAL INSTRUCTION *	Decoded as an illegal instruction
(16) or (32)	Indicates if the default code segment size is 16 or 32 bits. This is for fetch cycles only.

Hardware Display Format

In Hardware display format, the disassembler displays certain cycle type labels in parentheses. Table 2–3 shows these cycle type labels and gives a definition of the cycle they represent. Reads to interrupt and exception vectors will be labeled with the vector name.

Table 2–3: Cycle type definitions

Cycle type	Definition
(CO I/O RD)	A cycle reading data from an I/O port in the coprocessor
(CO I/O WR)	A cycle writing data to an I/O port in the coprocessor
(DMA CYCLE)	A direct memory access cycle
(EXTENSION)	A read cycle of either an extension long word or a word of an instruction
(FLUSH)	Instruction flushed from the pipeline
(HALT)	Address = 2 (Address bit 1 = 1)
(INT ACK)	An interrupt acknowledge cycle
(INVALID CYCLE)	An illegal cycle; an unrecognized combination of control group values
(I/O READ)	A cycle reading data from an I/O port
(I/O WRITE)	A cycle writing data to an I/O port
(LOCKED MEM READ)	Any locked cycle during which data is read from memory except: opcode fetch, extension, or interrupt acknowledge
(LOCKED MEM WRITE)	Any locked cycle during which data is written to memory
(MEM READ)	Any cycle during which data is read from memory except: opcode fetch, extension, or interrupt acknowledge
(MEM WRITE)	Any cycle during which data is written to memory
(RESERVED)	Any cycle during which the control group bit pattern indicates reserved
(RESET)	Latched reset signal asserted
(SHUTDOWN)	Address = 0

Figure 2–1 shows an example of the Hardware display.

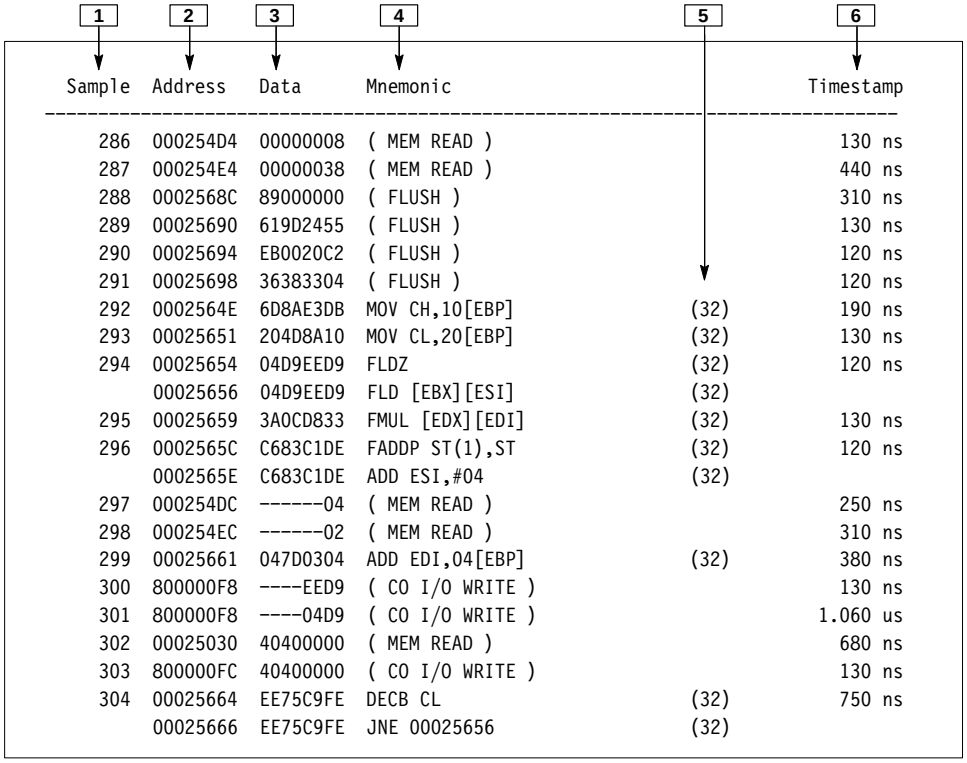


Figure 2–1: Hardware display

1 **Sample Column.** Lists the memory locations for the acquired data.

2 **Address Group.** Lists data from channels connected to the i386DX Address bus.

3 **Data Group.** Lists data from channels connected to the i386DX Data bus.

4 **Mnemonic Column.** Lists the disassembled instructions and cycle types.

5 This part of the mnemonic, (16) or (32), indicates that the fetch is from a 16- or 32-bit code segment size and disassembled accordingly.

6 **Timestamp.** Lists the timestamp values when a timestamp selection is made. Information on basic operations describes how you can select a timestamp.

Software Display Format

The Software display format shows only the first fetch of executed instructions. Flushed cycles and extensions are not shown, even though they are part of the executed instruction. Read extensions are used to disassemble the instruction, but are not displayed as a separate cycle in the Software display format. Data reads and writes are not displayed.

Control Flow Display Format

The Control Flow display format shows only the first fetch of instructions that change the flow of control.

Instructions that generate a change in the flow of control in the i386DX microprocessor are as follows:

CALL	INT	IRET	JMP	RET

Instructions that might generate a change in the flow of control in the i386DX microprocessor are as follows:

BOUND	JCXZ/JECXZ	JNE/JNZ	JP/JPE
DIV	JE/JZ	JNL/JGE	JS
IDIV	JL/JNGE	JNLE/JG	LOOP
INTO	JLE/JNG	JNO	LOOPNZ/LOOPNE
JB/JNAE/JC	JNB/JAE/JNC	JNP/JPO	LOOPZ/LOOPE
JBE/JNA	JNBE/JA	JNSJO	

Subroutine Display Format

The Subroutine display format shows only the first fetch of subroutine call and return instructions. It will display conditional subroutine calls if they are considered to be taken.

Instructions that generate a subroutine call or a return in the i386DX microprocessor are as follows:

BOUND	DIV	INT	IRET
CALL	IDIV	INTO	RET

Instructions that might generate a subroutine call or a return in the i386DX microprocessor are as follows:

CALLL	CALLS	RETL	RETS

Changing How Data is Displayed

There are fields and features that allow you to further modify displayed data to suit your needs. You can make selections unique to the i386DX support to do the following tasks:

- Change how data is displayed across all display formats
- Change the interpretation of disassembled cycles
- Display exception vectors

Optional Display Selections

You can make optional display selections for disassembled data to help you analyze the data. You can make these selections in the Disassembly property page (the Disassembly Format Definition overlay).

In addition to the common display options (described in the information on basic operations), you can change the displayed data in the following ways:

- Specify code segment size.
- Choose an interrupt table.
- Specify the starting address of the interrupt table.
- Specify the size of the interrupt table.

The i386DX support has four additional fields: Code Segment Size, Interrupt Table, Interrupt Table Address, and Interrupt Table Size. These fields appear in the area indicated in the information on basic operations.

Code Segment Size. You can select the default code size: 32 bit or 16 bit. The default code size is 16 bit.

Interrupt Table. You can specify if the interrupt table is Real, Virtual, or Protected. (Selecting Virtual is equivalent to selecting Protected.) The default is Real.

Interrupt Table Address. You can specify the starting address of the interrupt table in hexadecimal. The default starting address is 0x00000000.

Interrupt Table Size. You can specify the size of the interrupt table in hexadecimal. The default size is 0x400.

Marking Cycles

The disassembler has a Mark Opcode function that allows you to change the interpretation of a cycle type. Using this function, you can select a cycle and change it to one of the following cycle types:

- Opcode (the first word of an instruction)
- Extension (a subsequent word of an instruction)
- Flush (an opcode or extension that is fetched but not executed)
- Anything (any valid opcode, extension or flush)
- 16-bit or 32-bit default segment size

Mark selections for a 32-bit bus are as follows:

```
Any          Any          Any          OPCODE
Any          Any          OPCODE       Flush
Any          OPCODE       Flush        Flush
OPCODE       Flush        Flush        Flush
Ext          Ext          Ext          Ext
Flush        Flush        Flush        Flush

16-bit Default Segment Size
32-bit Default Segment Size

Undo marks on this cycle
```

Mark selections for a 16-bit bus are as follows:

```
Any          OPCODE
OPCODE       Any
Ext          Ext
Flush        Flush

16-bit Default Segment Size
32-bit Default Segment Size

Undo marks on this cycle
```

You can also use the Mark Opcode function to specify the default segment size mode (16 bit or 32 bit) for the cycle. The segment size selection changes the cycle the cursor is on and the remaining cycles to the end of memory or to the next mark.

Information on basic operations contains more details on marking cycles.

Displaying Exception Vectors

The disassembler can display i386DX exception vectors. You can select to display the interrupt vectors for Real, Virtual, or Protected mode in the Interrupt Table field. (Selecting Virtual is equivalent to selecting Protected.)

You can relocate the table by entering the starting address in the Interrupt Table Address field. The Interrupt Table Address field provides the disassembler with the offset address; enter an eight-digit hexadecimal value corresponding to the

offset of the base address of the exception table. The Interrupt Table Size field lets you specify a three-digit hexadecimal size for the table.

You can make these selections in the Disassembly property page (the Disassembly Format Definition overlay).

Table 2–4 lists the i386DX exception vectors for the Real Addressing mode.

Table 2–4: Interrupt vectors for Real Addressing mode

Exception number	Location in IV* table (in hexadecimal)	Displayed exception name
0	00	DIVIDE ERROR
1	04	DEBUG EXCEPTIONS
2	08	NMI INTERRUPT
3	0C	BREAKPOINT INTERRUPT
4	10	INTO DETECTED OVERFLOW
5	14	BOUND RANGE EXCEEDED
6	18	INVALID OPCODE
7	1C	COPROCESSOR NOT AVAILABLE
8	20	DOUBLE FAULT
9-11	24-2C	RESERVED
12	30	STACK EXCEPTION
13	34	SEGMENT OVERRUN
14-15	38-3C	RESERVED
16	40	COPROCESSOR MODE
17-31	44-7C	RESERVED
32-255	80-3FC	USER DEFINED

*** IV means interrupt vector.**

Table 2–5 lists the i386DX exception vectors for the Protected Addressing mode.

Table 2–5: Interrupt vectors for Protected Addressing mode

Exception number	Location in IDT* (in hexadecimal)	Displayed exception name
0	00	DIVIDE ERROR
1	08	DEBUG EXCEPTIONS
2	10	NMI INTERRUPT
3	18	BREAKPOINT INTERRUPT
4	20	INTO DETECTED OVERFLOW
5	28	BOUND RANGE EXCEEDED

Table 2–5: Interrupt vectors for Protected Addressing mode (cont.)

Exception number	Location in IDT* (in hexadecimal)	Displayed exception name
6	30	INVALID OPCODE
7	38	COPROCESSOR NOT AVAILABLE
8	40	DOUBLE FAULT
9	48	RESERVED
10	50	INVALID TSS
11	58	SEGMENT NOT PRESENT
12	60	STACK EXCEPTION
13	68	GENERAL PROTECTION
14	70	PAGE FAULT
15	78	RESERVED
16	80	COPROCESSOR ERROR
17-31	90-F8	RESERVED
32-255	100-7F8	USER DEFINED

*** IDT means interrupt descriptor table.**

Viewing an Example of Disassembled Data

A demonstration system file (or demonstration reference memory) is provided so you can see an example of how your i386DX microprocessor bus cycles and instruction mnemonics look when they are disassembled. Viewing the system file is not a requirement for preparing the module for use and you can view it without connecting the logic analyzer to your SUT.

Information on basic operations describes how to view the file.

Specifications

Specifications

This chapter contains the following information:

- Probe adapter description
- Specification tables
- Dimensions of the probe adapter
- Channel assignment tables
- Description of how the module acquires i386DX signals
- List of other accessible i386DX signals and extra acquisition channels

Probe Adapter Description

The probe adapter is a nonintrusive piece of hardware that allows the acquisition module to acquire data from an i386DX microprocessor in its own operating environment with little effect, if any, on that system. Information on basic operations contains a figure showing the logic analyzer connected to a typical probe adapter. Refer to that figure while reading the following description.

The probe adapter consists of a circuit board and a socket for an i386DX microprocessor. The probe adapter connects to the microprocessor in the SUT. Signals from the microprocessor-based system flow from the probe adapter to the channel groups and through the probe signal leads to the module.

All circuitry on the probe adapter is powered from the SUT.

Table 3–1 shows which microprocessors and their packages the TMS 104 supports.

Table 3–1: Supported microprocessors

Name	Package
Intel 80387DX	132-pin PGA
AMD 80386DX/DXL	132-pin PGA
AMD 80386DXL	132-pin PQFP

Configuration

The probe adapter does not require any configuration.

Specifications

In Table 3–2, for the 102/136-channel module, one podlet load is 20 kΩ in parallel with 2 pF. For the 96-channel module, one podlet load is 100 kΩ in parallel with 10 pF.

Table 3–2: Electrical specifications

Characteristics	Requirements	
SUT DC power requirements		
Voltage	4.75-5.25 VDC	
Current	I max (calculated) 610 mA I typ (measured) 395 mA	
SUT clock		
Clock rate	Min. 386DX 4MHz 386DXL 0 MHz Max. 386DX PGA 33 MHz 386DXL PGA 40 MHz 386DXL PQFP 25 MHz	
	Specification	
Minimum setup time required	**Probe adapter**	**386DX @ 40 MHz**
Data	4 ns	5 ns
HOLD	4 ns	11 ns
NA~, BS16~	4 ns	5 ns
All other signals	4 ns	See microprocessor spec.
	Specification	
Minimum hold time required	**Probe adapter**	**386DX @ 40 MHz**
Data	4 ns	3 ns (reads), 2 ns (writes)
HOLD	4 ns	2 ns
NA~, BS16~	4 ns	2 ns
All other signals	4 ns	See microprocessor spec.

Table 3–2: Electrical specifications (cont.)

Characteristics	Requirements	
	Specification	
Measured typical SUT signal loading	AC load	DC load
Address, Data, other signals	5 pF + 1 podlet	1 podlet
NMI, INTR, NA~, BS16~	12 pF + 1 podlet	16R8–5 in parallel with podlet
CLK2	7 pF	16R8–5 clock input
HLDS, ADS~, READY~, BE3~ – BE0~	12 pF + 1 podlet	1 podlet in parallel with 22V10C–10
Reset	19 pF	16R8–5 + 22V10C–10

Table 3–3 shows the environmental specifications.

Table 3–3: Environmental specification*

Characteristic	Description
Temperature	
Maximum operating	+50° C (+122° F)†
Minimum operating	0° C (+32° F)
Non-operating	–55° C to +75° C (–67° to +167° F)
Humidity	10 to 95% relative humidity
Altitude	
Operating	4.5 km (15,000 ft) maximum
Non-operating	15 km (50,000 ft) maximum
Electrostatic immunity	The probe adapter is static sensitive

* **Designed to meet Tektronix standard 062-2847-00 class 5.**

† **Not to exceed i386DX microprocessor thermal considerations. Forced air cooling might be required across the CPU.**

Table 3–4: Certifications and compliances

EC Compliance	There are no current European Directives that apply to this product.
Pollution Degree 2	Do not operate in environments where conductive pollutants might be present.

Figure 3–1 shows the dimensions of the PGA probe adapter. Information on basic operations shows the vertical clearance of the channel and clock probes when connected to a probe adapter in the description of general requirements and restrictions.

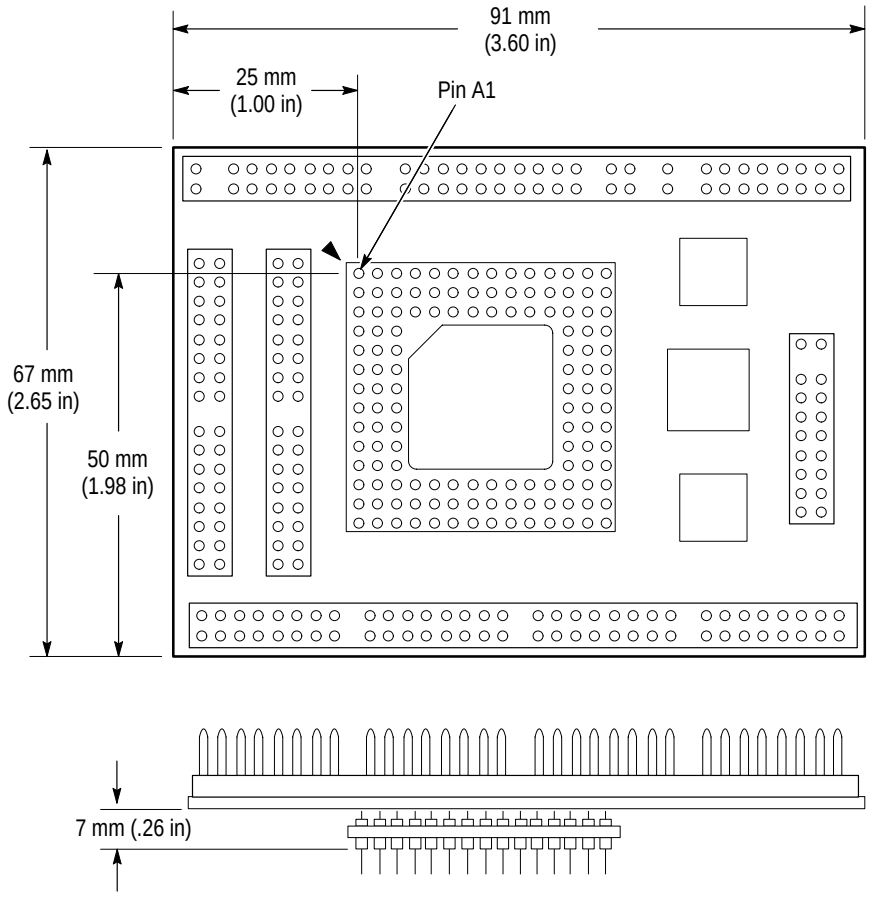


Figure 3–1: Minimum clearance of the PGA probe adapter

Figure 3–2 shows the dimensions of the PQFP probe adapter. Information on basic operations shows the vertical clearance of the channel and clock probes when connected to a probe adapter in the description of general requirements and restrictions.

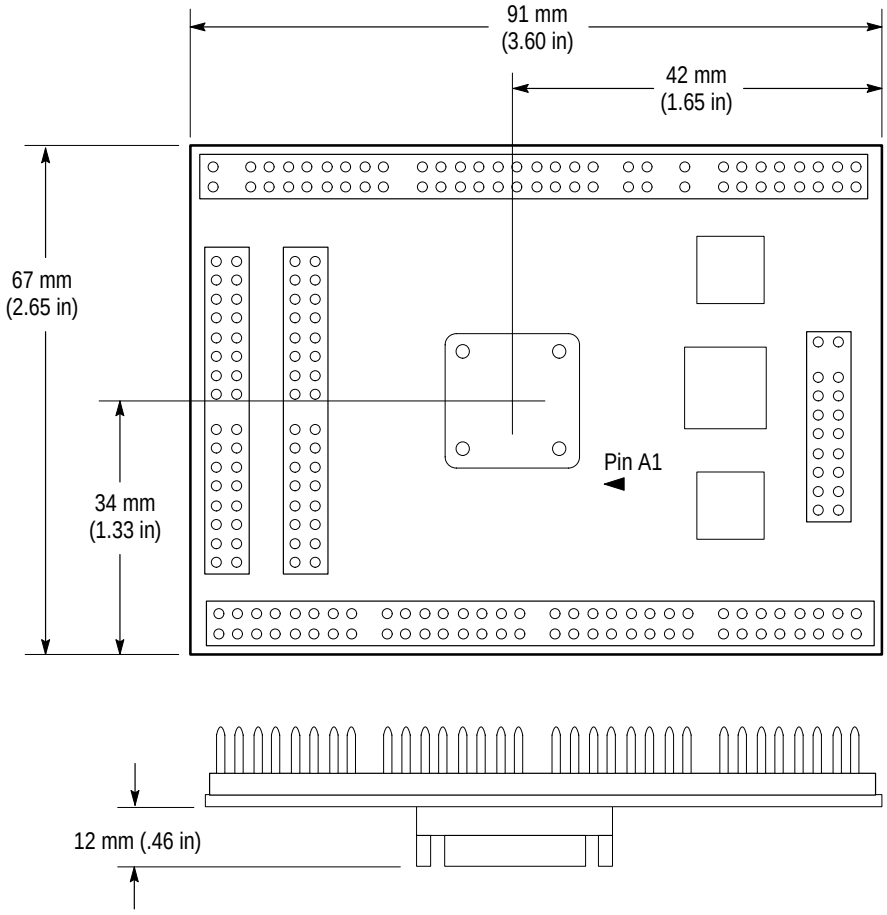


Figure 3–2: Minimum clearance of the PQFP probe adapter

Channel Assignments

Channel assignments shown in Table 3–5 through Table 3–13 use the following conventions:

- All signals are required by the support unless indicated otherwise.
- Channels are shown starting with the most significant bit (MSB) descending to the least significant bit (LSB).
- Channel group assignments are for the 102/136-channel, and 96-channel module unless otherwise noted.
- A tilde (~) following a signal name indicates an active low signal.

Table 3–5 shows the probe section and channel assignments for the Address group, and the microprocessor signal to which each channel connects. By default, this channel group is displayed in hexadecimal.

Table 3–5: Address group channel assignments

Bit order	Channel	i386DX signal name
31	A3:7	A31
30	A3:6	A30
29	A3:5	A29
28	A3:4	A28
27	A3:3	A27
26	A3:2	A26
25	A3:1	A25
24	A3:0	A24
23	A2:7	A23
22	A2:6	A22
21	A2:5	A21
20	A2:4	A20
19	A2:3	A19
18	A2:2	A18
17	A2:1	A17
16	A2:0	A16
15	A1:7	A15
14	A1:6	A14
13	A1:5	A13
12	A1:4	A12
11	A1:3	A11
10	A1:2	A10
9	A1:1	A9
8	A1:0	A8
7	A0:7	A7
6	A0:6	A6
5	A0:5	A5
4	A0:4	A4
3	A0:3	A3
2	A0:2	A2
1	A0:1	A1_D
0	A0:0	A0_D

Table 3–6 shows the section and channel assignments for the Data group, and the microprocessor signal to which each channel connects. By default, this channel group is displayed in hexadecimal.

Table 3–6: Data group channel assignments

Bit order	Channel	i386DX signal name
31	D3:7	D31
30	D3:6	D30
29	D3:5	D29
28	D3:4	D28
27	D3:3	D27
26	D3:2	D26
25	D3:1	D25
24	D3:0	D24
23	D2:7	D23
22	D2:6	D22
21	D2:5	D21
20	D2:4	D20
19	D2:3	D19
18	D2:2	D18
17	D2:1	D17
16	D2:0	D16
15	D1:7	D15
14	D1:6	D14
13	D1:5	D13
12	D1:4	D12
11	D1:3	D11
10	D1:2	D10
9	D1:1	D9
8	D1:0	D8
7	D0:7	D7
6	D0:6	D6
5	D0:5	D5
4	D0:4	D4
3	D0:3	D3
2	D0:2	D2
1	D0:1	D1
0	D0:0	D0

Table 3–7 shows the section and channel assignments for the Control group, and the microprocessor signal to which each channel connects. By default, this channel group is displayed symbolically.

Table 3–7: Control group channel assignments

Bit order	Channel	i386DX signal name
6	C2:3	RESET_L
5	C2:0	HLDA
4	C2:1	READY~
3	C3:5	LOCK~
2	C3:2	M/I0~
1	C3:3	D/C~
0	C3:4	W/R~

Table 3–8 shows the section and channel assignments for the DataSize group, and the microprocessor signal to which each channel connects. By default, this channel group is not visible.

Table 3–8: Datasize group channel assignments

Bit order	Channel	i386DX signal name
4	C3:6	BS16_L~
3	C3:0	BE3~
2	C2:7	BE2~
1	C2:6	BE1~
0	C2:4	BE0~

Table 3–9 shows the section and channel assignments for the Intr group, and the microprocessor signal to which each channel connects. By default, this channel group is not visible.

Table 3–9: Intr group channel assignments

Bit order	Channel	i386DX signal name
3	C0:4	NMI_L
2	C0:5	INTR_L
1	C1:1	NMI
0	C1:5	INTR

Table 3–10 shows the section and channel assignments for the Copr group, and the microprocessor signal to which each channel connects. By default, this channel group is not visible.

Table 3–10: Copr group channel assignments

Bit order	Channel	i386DX signal name
2	C0:1	BUSY~
1	C1:4	ERROR~
0	C1:0	PEREQ

Table 3–11 shows the section and channel assignments for the Misc group, and the microprocessor signal to which each channel connects. By default, this channel group is not visible.

Table 3–11: Misc group channel assignments

Bit order	Channel	i386DX signal name
3	C2:5	CLK
2	C2:2	ADS~
1	C3:7	NA_L~
0	C3:1	PIPE

Table 3–12 shows the section and channel assignments for the Misc2 group, and the microprocessor signal to which each channel connects. By default, this channel group is not visible.

Table 3–12: Misc2 group channel assignments

Bit order	Channel	i386DX signal name
3	C0:6	RESET
2	C0:0	HOLD

Table 3–12: Misc2 group channel assignments

Bit order	Channel	i386DX signal name
1	C0:3	NA~
0	C0:2	BS16~

Table 3–13 shows the channel assignments for the clock channels (not part of any group), and the microprocessor signal to which each channel connects.

Table 3–13: Clock channel assignments

Channel	i386DX signal name
CLK3	PIPE
CLK2	CLK
CLK1	NA_L~
CLK0	BS16_L~

These channels are used only to clock in data; they are not acquired or displayed. To acquire data from any of the signals shown in Table 3–13, you must connect another channel probe to the signal, called double probing.

How Data is Acquired

This part of this section explains how the module acquires i386DX signals using the TMS 104 support and probe adapter. This part also provides additional information on microprocessor signals accessible on or not accessible on the probe adapter, and on extra acquisition channels available for you to use for additional connections.

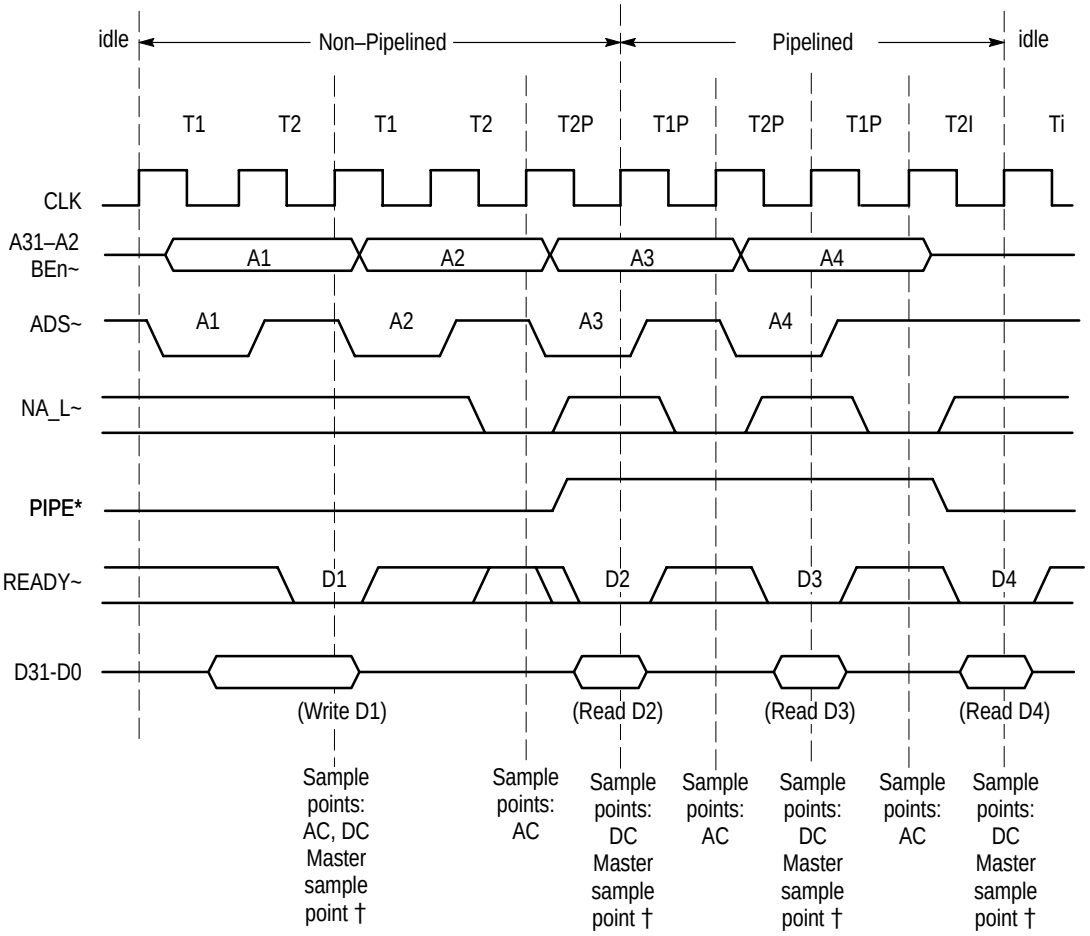
Custom Clocking

A special clocking program is loaded to the module every time you load the 386DX support. This special clocking is called Custom.

With Custom clocking, the module logs in signals from multiple groups of channels at different times as they become valid on the i386DX bus. The module then sends all the logged-in signals to the trigger machine and to the acquisition memory of the module for storage.

In Custom clocking, the module clocking state machine (CSM) generates one master sample for each microprocessor bus cycle, no matter how many clock cycles are contained in the bus cycle.

Figure 3–3 shows when the various sample points are asserted. Sample point AC is at the end of a valid address assertion in order to maximize setup time. Sample points DC and M occur at the end of a bus cycle, the only time the data is valid.



AC = NA_L~, BS16_L~, W/R~, D/C~, M/IO~, BE3~–BE0~, RESET_L~, ADS~, HLDA, C1:7, C1:6, C1:3, C1:2, C0:7, RESET, NA~, BS16~, A31–A2

DC = LOCK~, PIPE, CLK, READY~, INTR, ERROR~, NMI, PEREQ, INTR_L, NMI_L, BUSY~, HOLD, D31–D0

†Channels not set up in a channel group by the TMS 104 software are logged with the Master sample.

Figure 3–3: i386DX bus timing (non-pipelined and pipelined)

Clocking Options

The clocking algorithm for the i386DX support has two variations: DMA Cycles Excluded, and DMA Cycles Included.

DMA Cycles Excluded. Whenever the HLDA signal is high, no bus cycles are logged in. Only bus cycles driven by the i386DX microprocessor (HLDA low) will be logged in.

DMA Cycles Included. All bus cycles, including DMA cycles, are logged in.

When the HLDA signal is high, the i386DX microprocessor has given up the bus to an alternate device. The design of the i386DX system affects what data will be logged in. The only samples the data at the pins of the i386DX microprocessor. To properly log in bus activity, any buffers between the i386DX microprocessor and the alternate bus master must be enabled and pointing at the i386DX microprocessor.

There are three possible i386DX system designs and clocking interactions when an alternate bus master has control of the bus. The three different possibilities are listed below (in each case, the HLDA signal is logged in as a high level):

- If the DMA drives the same control lines as the i386DX microprocessor, and the i386DX microprocessor "sees" these signals, the bus activity is logged in like normal bus cycles except that the HLDA signal is high.
- If none of the control lines are driven or if the i386DX microprocessor can not see them, the will still clock in an DMA cycle. The information on the bus, one clock prior to the HLDA signal going low, is logged in. If the ADS# signal goes low on the same clock when the HLDA signal goes low, the address that gets logged in will be the "next address," not the address that occurred one clock before the HLDA signal went low.
- If some of the i386DX microprocessor control lines are visible (but not all), the logs in what it determines is valid from the control signals and logs in the remaining bus signals one clock cycle prior to the HLDA signal going low. If the ADS# signal goes low on the same clock that the HLDA signal goes low, the "next address" will be logged in instead of the previously saved address.

Alternate Microprocessor Connections

You can connect to microprocessor signals that are not required by the support so you can do more advanced timing analysis. For a list of signals required or not required for disassembly, refer to the channel assignment tables beginning on page 3–6.

Remember that these channels are already included in a channel group. If you do connect these channels to other signals, you should set up another channel group for them.

Signals On the Probe Adapter

All i386DX microprocessor signals are accessible on the probe adapter.

Extra Channels

Table 3–14 lists extra sections and channels that are left after you have connected all the probes used by the support. You can use these extra channels to make alternate SUT connections, and they will be logged in at the same time data is valid (READY# asserted). You can use these extra channels to make alternate SUT connections.

Table 3–14: Extra module sections and channels

Module	Section: channels
102-channels	C1:7, C1:6, C1:3, C1:2, C0:7
136-channels	C1:7, C1:6, C1:3, C1:2, C0:7, E3:7-0, E2:7-0, E1:7-0, E0:7-0
96-channels	C1:7, C1:6, C1:3, C1:2, C0:7

These channels are not defined in any channel group and data acquired from them is not displayed. To display data, you will need to define a channel group.

WARNING

The following servicing instructions are for use only by qualified personnel. To avoid injury, do not perform any servicing other than that stated in the operating instructions unless you are qualified to do so. Refer to all Safety Summaries before performing any service.

Maintenance

Maintenance

This section contains information on the following topics:

- Probe adapter circuit description
- How to replace a signal lead
- How to replace a protective socket

Probe Adapter Circuit Description

The active circuitry on the probe consists of three PALs: two 16R8–5s and one 22V10C–10. The first 16R8–5 PAL divides the clock frequency in half. This divided clock is then used to drive the remaining two PALs.

The second 16R8–5 PAL synchronizes most of the asynchronous inputs, and brings them into time alignment with the other signals, so that a single edge of the clock is sufficient for all.

The 22V10C–10 PAL (referred to as the T-state tracking PAL) is used to implement a state machine that tracks the bus states of the 386DX. This PAL synthesizes a signal called PIPE, which is used as a clock qualifier. PIPE informs the clocking state machine when the 386DX is in pipelined bus mode. The times for sampling the address vary as a function of pipelined operation, which can change dynamically and is not self-evident (thus the need for the PAL). The –10 speed supports microprocessors with speeds up to 50 MHz.

J1771 and J1671 are used to turn off the cache. The SUT drives these lines, therefore the SUT driver must be disabled to use this option.

Replacing Signal Leads

Information on basic operations describes how to replace signal leads (individual channel and clock probes).

Replacing Protective Sockets

Information on basic operations describes how to replace protective sockets.

Replaceable Electrical Parts

Replaceable Electrical Parts

This chapter contains a list of the replaceable electrical components for the TMS 104 i386DX microprocessor support. Use this list to identify and order replacement parts.

Parts Ordering Information

Replacement parts are available through your local Tektronix field office or representative.

Changes to Tektronix products are sometimes made to accommodate improved components as they become available and to give you the benefit of the latest improvements. Therefore, when ordering parts, it is important to include the following information in your order:

- Part number
- Instrument type or model number
- Instrument serial number
- Instrument modification number, if applicable

If you order a part that has been replaced with a different or improved part, your local Tektronix field office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

Using the Replaceable Electrical Parts List

The tabular information in the Replaceable Electrical Parts List is arranged for quick retrieval. Understanding the structure and features of the list will help you find all of the information you need for ordering replacement parts. The following table describes each column of the electrical parts list.

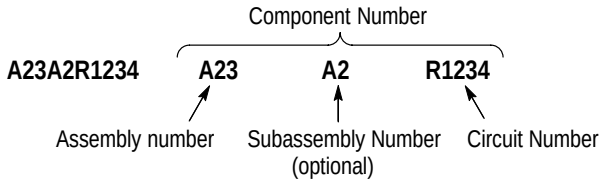
Parts list column descriptions

Column	Column name	Description
1	Component number	The component number appears on diagrams and circuit board illustrations, located in the diagrams section. Assembly numbers are clearly marked on each diagram and circuit board illustration in the *Diagrams* section, and on the mechanical exploded views in the *Replaceable Mechanical Parts* list section. The component number is obtained by adding the assembly number prefix to the circuit number (see Component Number illustration following this table). The electrical parts list is arranged by assemblies in numerical sequence (A1, with its subassemblies and parts, precedes A2, with its subassemblies and parts). Chassis-mounted parts have no assembly number prefix, and they are located at the end of the electrical parts list.
2	Tektronix part number	Use this part number when ordering replacement parts from Tektronix.
3 and 4	Serial number	Column three indicates the serial number at which the part was first effective. Column four indicates the serial number at which the part was discontinued. No entry indicates the part is good for all serial numbers.
5	Name & description	An item name is separated from the description by a colon (:). Because of space limitations, an item name may sometimes appear as incomplete. Use the U.S. Federal Catalog handbook H6-1 for further item name identification.
6	Mfr. code	This indicates the code number of the actual manufacturer of the part.
7	Mfr. part number	This indicates the actual manufacturer's or vendor's part number.

Abbreviations

Abbreviations conform to American National Standard ANSI Y1.1–1972.

Component Number



Read: Resistor 1234 (of Subassembly 2) of Assembly 23

List of Assemblies

A list of assemblies is located at the beginning of the electrical parts list. The assemblies are listed in numerical order. When a part's complete component number is known, this list will identify the assembly in which the part is located.

Chassis Parts

Chassis-mounted parts and cable assemblies are located at the end of the Replaceable Electrical Parts List.

Mfr. Code to Manufacturer Cross Index

The table titled Manufacturers Cross Index shows codes, names, and addresses of manufacturers or vendors of components listed in the parts list.

Manufacturers cross index

Mfr. code	Manufacturer	Address	City, state, zip code
TK0875	MATSUO ELECTRONICS INC	831 S DOUBLAS ST	EL SEGUNDO CA 92641
TK2058	TDK CORPORATION OF AMERICA	1600 FEEHANVILLE DRIVE	MOUNT PROSPECT, IL 60056
53387	3M COMPANY ELECTRONIC PRODUCTS DIV	3M AUSTIN CENTER	AUSTIN TX 78769–2963
63058	MCKENZIE TECHNOLOGY	910 PAGE AVENUE	FREMONT CA 94538
80009	TEKTRONIX INC	14150 SW KARL BRAUN DR PO BOX 500	BEAVERTON OR 97077–0001

Replaceable electrical parts list

Component number	Tektronix part number	Serial no. effective	Serial no. discont'd	Name & description	Mfr. code	Mfr. part number
A1	671–2336–XX			CIRCUIT BD ASSY:80386DX PROBE ADAPTER;PGA132	80009	6712336XX
A2	671–2467–XX			CIRCUIT BD ASSY:80386DX PQFP132 SOLDERED,PROBE ADAPTER;	80009	6712467XX
A1	671–2336–XX			CIRCUIT BD ASSY:80386DX PROBE ADAPTER;PGA132	80009	6712336XX
A1C120	283–5003–00			CAP,FXD,CERAMIC:MLC;0.01UF,10%,50V,X7R,1206	TK2058	C3216X7R1H103K–
A1C150	283–5003–00			CAP,FXD,CERAMIC:MLC;0.01UF,10%,50V,X7R,1206	TK2058	C3216X7R1H103K–
A1C220	283–5004–00			CAP,FXD,CERAMIC:MLC;0.1UF,10%,25V,X7R,1206	TK2058	C3216X7R1E104K–
A1C230	283–5004–00			CAP,FXD,CERAMIC:MLC;0.1UF,10%,25V,X7R,1206	TK2058	C3216X7R1E104K–
A1C240	283–5004–00			CAP,FXD,CERAMIC:MLC;0.1UF,10%,25V,X7R,1206	TK2058	C3216X7R1E104K–
A1C250	290–5005–00			CAP,FXD,TANT:47UF,10%,10V,5.8MM X 4.6MM	TK0875	267M–1002–476–K
A1C320	283–5004–00			CAP,FXD,CERAMIC:MLC;0.1UF,10%,25V,X7R,1206	TK2058	C3216X7R1E104K–
A1C330	283–5004–00			CAP,FXD,CERAMIC:MLC;0.1UF,10%,25V,X7R,1206	TK2058	C3216X7R1E104K–
A1C340	283–5004–00			CAP,FXD,CERAMIC:MLC;0.1UF,10%,25V,X7R,1206	TK2058	C3216X7R1E104K–
A1C420	283–5003–00			CAP,FXD,CERAMIC:MLC;0.01UF,10%,50V,X7R,1206	TK2058	C3216X7R1H103K–
A1C440	283–5004–00			CAP,FXD,CERAMIC:MLC;0.1UF,10%,25V,X7R,1206	TK2058	C3216X7R1E104K–
A1C450	283–5003–00			CAP,FXD,CERAMIC:MLC;0.01UF,10%,50V,X7R,1206	TK2058	C3216X7R1H103K–
A1J100	————————			CONN,HDR:PCB;MALE,STR,2 X 40,0.1 CTR,0.235 (SEE RMPL FIG.1)		
A1J130	————————			CONN,HDR:PCB;MALE,STR,2 X 40,0.1 CTR,0.235 (SEE RMPL FIG.1)		
A1J140	————————			CONN,HDR:PCB;MALE,STR,2 X 40,0.1 CTR,0.235 (SEE RMPL FIG.1)		
A1J150	————————			CONN,HDR:PCB;MALE,STR,2 X 40,0.1 CTR,0.235 (SEE RMPL FIG.1)		
A1J200	————————			CONN,HDR:PCB;MALE,STR,2 X 40,0.1 CTR,0.235 (SEE RMPL FIG.1)		
A1J220	————————			CONN,HDR:PCB;MALE,STR,2 X 40,0.1 CTR,0.235 (SEE RMPL FIG.1)		
A1J300	————————			CONN,HDR:PCB;MALE,STR,2 X 40,0.1 CTR,0.235 (SEE RMPL FIG.1)		
A1J320	————————			CONN,HDR:PCB;MALE,STR,2 X 40,0.1 CTR,0.235 (SEE RMPL FIG.1)		
A1J350	————————			CONN,HDR:PCB;MALE,STR,2 X 40,0.1 CTR,0.235 (SEE RMPL FIG.1)		
A1J400	————————			CONN,HDR:PCB;MALE,STR,2 X 40,0.1 CTR,0.235 (SEE RMPL FIG.1)		
A1J420	————————			CONN,HDR:PCB;MALE,STR,2 X 40,0.1 CTR,0.235 (SEE RMPL FIG.1)		
A1J440	————————			CONN,HDR:PCB;MALE,STR,2 X 40,0.1 CTR,0.235 (SEE RMPL FIG.1)		
A1J450	————————			CONN,HDR:PCB;MALE,STR,2 X 40,0.1 CTR,0.235 (SEE RMPL FIG.1)		
A1U240	160–8855–00			IC,DIGITAL:STTL,PLD;PAL,16R8,5NS,210MA,LATCH	80009	160–8855–00

Replaceable electrical parts list (cont.)

Component number	Tektronix part number	Serial no. effective	Serial no. discont'd	Name & description	Mfr. code	Mfr. part number
A1U330	————————			SOCKET,PGA:PCB;132 POS,14 X 14,0.1 CTR,0.170 H X 0.275 TAIL,OPEN CTR,SYMMETRICAL,PAT (SEE RMPL FIG.1)		
A1U340	160–8854–00			IC,DIGITAL:CMOS,PLD;PAL,22V10,10NS,180MA,386 DX 'TRACKING'	80009	160–8854–00
A1U440	160–8837–00			IC,DIGITAL:STTL,PLD;PAL,16R8,5NS,210MA,CLOCK–DIV	80009	160–8837–00
A2	671–2467–XX			CIRCUIT BD ASSY:80386DX PQFP132 SOLDERED,PROBE ADAPTER;	80009	6712467XX
A2C120	283–5003–00			CAP,FXD,CERAMIC:MLC;0.01UF,10%,50V,X7R,1206	TK2058	C3216X7R1H103K–
A2C150	283–5003–00			CAP,FXD,CERAMIC:MLC;0.01UF,10%,50V,X7R,1206	TK2058	C3216X7R1H103K–
A2C220	283–5004–00			CAP,FXD,CERAMIC:MLC;0.1UF,10%,25V,X7R,1206	TK2058	C3216X7R1E104K–
A2C230	283–5004–00			CAP,FXD,CERAMIC:MLC;0.1UF,10%,25V,X7R,1206	TK2058	C3216X7R1E104K–
A2C240	283–5004–00			CAP,FXD,CERAMIC:MLC;0.1UF,10%,25V,X7R,1206	TK2058	C3216X7R1E104K–
A2C250	290–5005–00			CAP,FXD,TANT:47UF,10%,10V,5.8MM X 4.6MM	TK0875	267M–1002–476–K
A2C320	283–5004–00			CAP,FXD,CERAMIC:MLC;0.1UF,10%,25V,X7R,1206	TK2058	C3216X7R1E104K–
A2C330	283–5004–00			CAP,FXD,CERAMIC:MLC;0.1UF,10%,25V,X7R,1206	TK2058	C3216X7R1E104K–
A2C340	283–5004–00			CAP,FXD,CERAMIC:MLC;0.1UF,10%,25V,X7R,1206	TK2058	C3216X7R1E104K–
A2C420	283–5003–00			CAP,FXD,CERAMIC:MLC;0.01UF,10%,50V,X7R,1206	TK2058	C3216X7R1H103K–
A2C440	283–5004–00			CAP,FXD,CERAMIC:MLC;0.1UF,10%,25V,X7R,1206	TK2058	C3216X7R1E104K–
A2C450	283–5003–00			CAP,FXD,CERAMIC:MLC;0.01UF,10%,50V,X7R,1206	TK2058	C3216X7R1H103K–
A2J100	————————			CONN,HDR:PCB;MALE,STR,2 X 40,0.1 CTR,0.235 (SEE RMPL FIG.2)		
A2J130	————————			CONN,HDR:PCB;MALE,STR,2 X 40,0.1 CTR,0.2355 (SEE RMPL FIG.2)		
A2J140	————————			CONN,HDR:PCB;MALE,STR,2 X 40,0.1 CTR,0.2355 (SEE RMPL FIG.2)		
A2J150	————————			CONN,HDR:PCB;MALE,STR,2 X 40,0.1 CTR,0.2355 (SEE RMPL FIG.2)		
	————————					
A2J200	————————			CONN,HDR:PCB;MALE,STR,2 X 40,0.1 CTR,0.2355 (SEE RMPL FIG.2)		
A2J220	————————			CONN,HDR:PCB;MALE,STR,2 X 40,0.1 CTR,0.2355 (SEE RMPL FIG.2)		
A2J300	————————			CONN,HDR:PCB;MALE,STR,2 X 40,0.1 CTR,0.2355 (SEE RMPL FIG.2)		
A2J320	————————			CONN,HDR:PCB;MALE,STR,2 X 40,0.1 CTR,0.2355 (SEE RMPL FIG.2)		
A2J350	————————			CONN,HDR:PCB;MALE,STR,2 X 40,0.1 CTR,0.2355 (SEE RMPL FIG.2)		
	————————					
A2J400	————————			CONN,HDR:PCB;MALE,STR,2 X 40,0.1 CTR,0.2355 (SEE RMPL FIG.2)		
A2J420	————————			CONN,HDR:PCB;MALE,STR,2 X 40,0.1 CTR,0.2355 (SEE RMPL FIG.2)		
A2J440	————————			CONN,HDR:PCB;MALE,STR,2 X 40,0.1 CTR,0.2355 (SEE RMPL FIG.2)		
A2J450	————————			CONN,HDR:PCB;MALE,STR,2 X 40,0.1 CTR,0.2355 (SEE RMPL FIG.2)		

Replaceable electrical parts list (cont.)

Component number	Tektronix part number	Serial no. effective	Serial no. discont'd	Name & description	Mfr. code	Mfr. part number
A2P330	————————			CLIP,ELECTRICAL:ASSEMBLY,PQFP1325 (SEE RMPL FIG.2)		
A2U240	160–8855–00			IC,DIGITAL:STTL,PLD;PAL,16R8,5NS,210MA,LATCH	80009	160–8855–00
A2U340	160–8854–00			IC,DIGITAL:CMOS,PLD;PAL,22V10,10NS,180MA,386 DX 'TRACKING'	80009	160–8854–00
A2U440	160–8837–00			IC,DIGITAL:STTL,PLD;PAL,16R8,5NS,210MA,CLOCK–DIV	80009	160–8837–00

Replaceable Mechanical Parts

Replaceable Mechanical Parts

This chapter contains a list of the replaceable mechanical components for the TMS 104 i386DX microprocessor support. Use this list to identify and order replacement parts.

Parts Ordering Information

Replacement parts are available through your local Tektronix field office or representative.

Changes to Tektronix products are sometimes made to accommodate improved components as they become available and to give you the benefit of the latest improvements. Therefore, when ordering parts, it is important to include the following information in your order:

- Part number
- Instrument type or model number
- Instrument serial number
- Instrument modification number, if applicable

If you order a part that has been replaced with a different or improved part, your local Tektronix field office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

Using the Replaceable Mechanical Parts List

The tabular information in the Replaceable Mechanical Parts List is arranged for quick retrieval. Understanding the structure and features of the list will help you find all of the information you need for ordering replacement parts. The following table describes the content of each column in the parts list.

Parts list column descriptions

Column	Column name	Description
1	Figure & index number	Items in this section are referenced by figure and index numbers to the exploded view illustrations that follow.
2	Tektronix part number	Use this part number when ordering replacement parts from Tektronix.
3 and 4	Serial number	Column three indicates the serial number at which the part was first effective. Column four indicates the serial number at which the part was discontinued. No entries indicates the part is good for all serial numbers.
5	Qty	This indicates the quantity of parts used.
6	Name & description	An item name is separated from the description by a colon (:). Because of space limitations, an item name may sometimes appear as incomplete. Use the U.S. Federal Catalog handbook H6-1 for further item name identification.
7	Mfr. code	This indicates the code of the actual manufacturer of the part.
8	Mfr. part number	This indicates the actual manufacturer's or vendor's part number.

Abbreviations

Abbreviations conform to American National Standard ANSI Y1.1–1972.

Chassis Parts

Chassis-mounted parts and cable assemblies are located at the end of the Replaceable Electrical Parts List.

Mfr. Code to Manufacturer Cross Index

The table titled Manufacturers Cross Index shows codes, names, and addresses of manufacturers or vendors of components listed in the parts list.

Manufacturers cross index

Mfr. code	Manufacturer	Address	City, state, zip code
TK2548	XEROX BUSINESS SERVICES DIV OF XEROX CORPORATION	14181 SW MILLIKAN WAY	BEAVERTON OR 97077
53387	3M COMPANY ELECTRONIC PRODUCTS DIV	3M AUSTIN CENTER	AUSTIN TX 78769–2963
80009	TEKTRONIX INC	14150 SW KARL BRAUN DR PO BOX 500	BEAVERTON OR 97077–0001

Replaceable mechanical parts list

Fig. & index number	Tektronix part number	Serial no. effective	Serial no. discont'd	Qty	Name & description	Mfr. code	Mfr. part number
1–0	010-0532-00			1	PROBE ADAPTER:80386DX,PGA132,SOCKETED	80009	010-0532-00
–1	131-5267-00			3	CONN,HDR:PCB;MALE,STR,2 X 40,0.1 CTR,0.235 MLG X 0.110 TAIL,30GOLD (J100,J130,J140,J150,J200,J220,J300,J320,J350,J400,J420, J440,J450)	53387	2480-6122–TB
–2	671-2336-00			1	CIRCUIT BD ASSY:80386DX PROBE ADAPTER;PGA132 (A01)	80009	671-2336-00
–3	136-0940-00			2	SOCKET,PGA:PCB;132 POS,14 X 14.0.1 CTR	63058	136-0940-00
					STANDARD ACCESSORIES		
	070-9807-00			1	MANUAL,TECH:INSTRUCTION,i386DX,DISSASEMBLER, TMS 104	80009	070-9807-00
	070–9803–00			1	MANUAL, TECH:TLA 700 SERIES MICRO SUPPORT INSTALLATION	80009	070–9803–00
					OPTIONAL ACCESSORIES		
	070-9802-00			1	MANUAL, TECH:BASIC OPS MICRO SUP ON DAS/TLA 500 SERIES LOGIC ANALYZERS	80009	070-9802-00

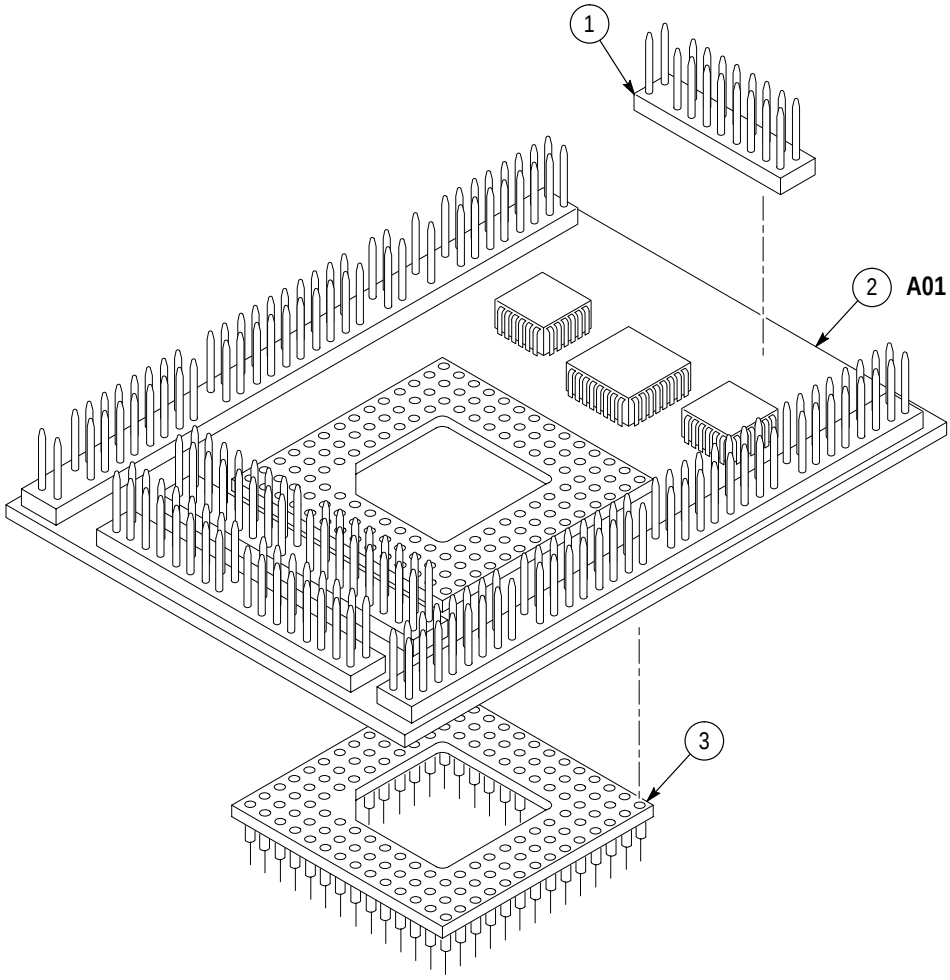


Figure 1: i386DX PGA probe adapter exploded view

Replaceable mechanical parts list

Fig. & index number	Tektronix part number	Serial no. effective	Serial no. discont'd	Qty	Name & description	Mfr. code	Mfr. part number
2–1	131-5267-00			4	CONN,HDR:PCB;MALE,STR,2 X 40,0.1 CTR,0.235 MLG X 0.110 TAIL,30GOLD (J100,J130,J140,J150,J200,J220J300,J320,J350,J400,J420, J440,J450)	53387	2480-6122-TB
–2	671-2467-00			1	CIRCUIT BD ASSY:80386DX PQFP132 SOLDERED,PROBE ADAPTER;	80009	671-2467-00
					STANDARD ACCESSORIES		
	070-9807-00			1	MANUAL,TECH:INSTRUCTION,i386DX,DISSASEMBLER, TMS 104	80009	070-9807-00
	070–9803–00			1	MANUAL, TECH:TLA 700 SERIES MICRO SUPPORT INSTALLATION	80009	070–9803–00
					OPTIONAL ACCESSORIES		
	070-9802-00			1	MANUAL, TECH:BASIC OPS MICRO SUP ON TLA 500 SERIES & DAS LOGIC ANALYZERS	80009	070-9802-00

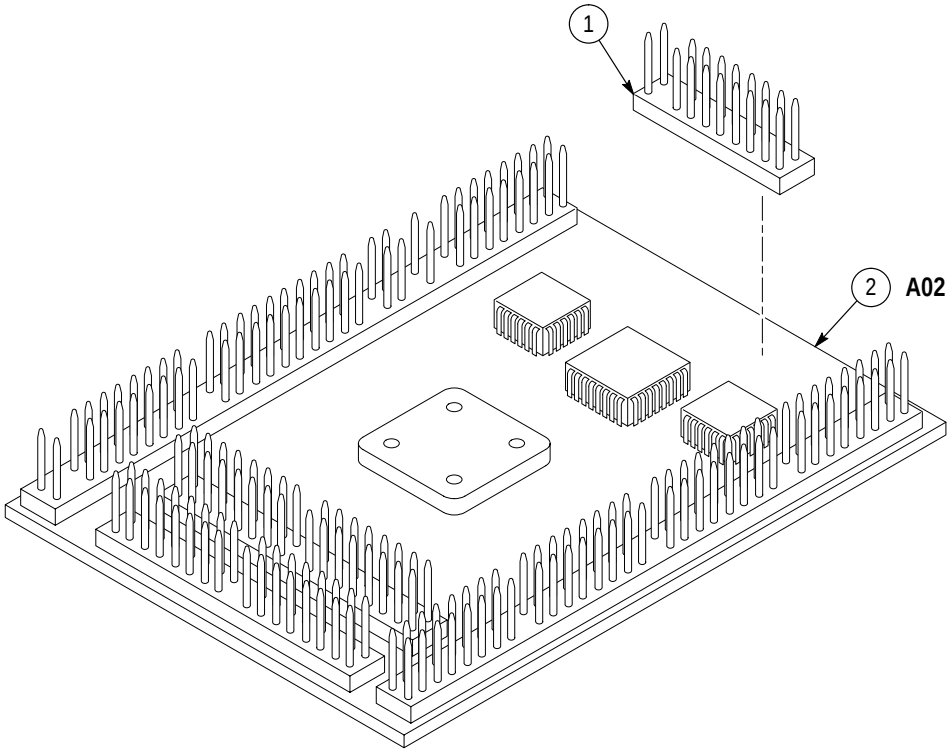


Figure 2: i386DX PQFP probe adapter exploded view

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